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| 09/640,118 | 08/16/2000 | G. Glenn Henry | CNTR:1356 | 4572 |

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| EXAMINER | |
|---|---|
| LI, AIMEE J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 7 |

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/640,118 | HENRY ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-19 and 21-24 have been considered. Claims 1, 3-6, 11, 13, 18, and 21 have been amended as per Applicant's request. Claim 20 has been cancelled as per Applicant's request.

### *Amendment Non-compliance*

2. Applicant's amendment fails to comply with the revised 37 CFR 1.121, which is required as of July 30, 2003. More specifically, applicant has used status identifier "Original" for claim 6. However, claim 6 has been amended and should have the status identifier "Presently Amended". In the future, the examiner will send out a notice of non-compliant amendment for failure to comply with the revised 37 CFR 1.121. Please see the attached flyer for more details.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-19 and 21-24 are rejected under 35 U.S.C. 102(b) as being taught by Bosshart, U.S. Patent Number 5,235,686 (herein referred to as Bosshart).

5. Referring to claim 1, Bosshart has taught an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12;

column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8), the apparatus comprising:

a. Instruction translation logic, configured to retrieve macro instructions provided via the external instruction bus, and configured to decode each of said macro instructions into associated native instructions for execution by the microprocessor, wherein said instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8); and

b. Bypass logic, coupled to said instruction translation logic, configured to disable said instruction translation logic upon detection of said native bypass macro instruction, and configured to provide the programmed native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

6. Referring to claim 2, Bosshart has taught wherein the programmed native instructions are provided from a memory to the external instruction bus (Rosshart column 1, lines 17-37; column

1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

7. Referring to claim 3, Bosshart has taught wherein execution of said native bypass macro instruction causes the microprocessor to transfer program control to the programmed native instructions (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

8. Referring to claim 4, Bosshart has taught wherein said bypass logic comprises mode detection logic, configured to detect said native bypass macro instruction within a macro instruction sequence that is provided to said instruction translation logic, wherein, upon detection of said native bypass macro instruction, said mode detection logic directs said instruction translation logic to cease decoding said macro instruction sequence following decoding of said native bypass macro instruction (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

9. Referring to claim 5, Bosshart has taught wherein said unconditional jump native instruction directs the microprocessor to transfer program control to said memory address (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

10. Referring to claim 6, Bosshart has taught where said memory address is provided in an architectural register (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

11. Referring to claim 7, Bosshart has taught wherein said bypass logic further comprises a native instruction router, coupled to said mode detection logic, configured to receive the programmed native instructions, and configured to route the programmed native instructions to a native instruction bus (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

12. Referring to claim 8, Bosshart has taught wherein, said mode detection logic is also configured to detect a native branch return macro instruction, said native branch return macro instruction following the programmed native instructions, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said instruction translation logic to resume decoding said macro instruction sequence (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

13. Referring to claim 9, Bosshart has taught wherein said instruction translation logic decodes said native branch return macro instruction into a native branch return native instruction, and wherein said native branch return native instruction directs the microprocessor to transfer program control to a return address (Rosshart column 1, lines 17-37; column 1, line 53 to column

2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

14. Referring to claim 10, Bosshart has taught wherein said return address designates a next macro instruction, said next macro instruction being within said macro instruction sequence and following said native branch macro instruction (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

15. Referring to claim 11, Bosshart has taught an apparatus, for allowing a micro instruction to be directly provided from an external instruction bus to execution logic within a pipeline microprocessor (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8), the apparatus comprising:

a. A translator, for receiving macro instructions from a macro instruction bus, and for translating each of said macro instructions into associated micro instructions, said associated micro instructions being provided to the execution logic via a micro instruction bus, wherein said translator translates a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the micro instruction (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to

column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8); and

b. Bypass logic, coupled to said translator, for routing the micro instruction to the execution logic (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8), said bypass logic comprising:

i. A mode detector, for detecting said native bypass macro instruction, and for directing that said translator cease instruction translation (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8); and

ii. Native instruction routing logic, coupled to said mode detector, for receiving said micro instruction from said macro instruction bus, and for providing said micro instruction to said micro instruction bus, thereby circumventing said translator (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

16. Referring to claim 12, Bosshart has taught wherein the external instruction bus typically provides said macro instructions to the microprocessor (Rosshart column 1, lines 17-37; column

1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

17. Referring to claim 13, Bosshart has taught wherein the execution logic executes said unconditional jump native instruction by transferring program control to said memory address that contains the micro instruction (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

18. Referring to claim 14, Bosshart has taught wherein said memory address is provided in an architectural register (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

19. Referring to claim 15, Bosshart has taught wherein, said mode detector is configured to detect a native branch return macro instruction, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said translator to resume instruction translation (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

20. Referring to claim 16, Bosshart has taught wherein the execution logic executes said native branch return macro instruction by transferring program control to a return memory address (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line

46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

21. Referring to claim 17, Bosshart has taught wherein said return memory address contains a next macro instruction (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

22. Referring to claim 18, Bosshart has taught a microprocessor for executing micro instructions directly from memory, the microprocessor comprising:

a. Translation logic, for receiving macro instructions from the memory, and for decoding said macro instructions into corresponding micro instructions for execution by the microprocessor (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8);

b. Mode detection logic, coupled to said translation logic, for detecting bypass macro instructions, and for directing the microprocessor to execute the micro instructions directly from the memory rather than via said translation logic (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8), said bypass macro instructions comprising:

i. A native branch macro instruction, directing that program control be transferred to a target address, wherein said translation logic decodes said native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to said target address, and wherein said target address contains the micro instructions; (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8) and

ii. A native branch return macro instruction, directing that program control be transferred to a return address (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8); and

iii. An instruction router, coupled to said mode detection logic, for receiving the micro instructions, and for routing the micro instructions to execution logic, thereby bypassing said translation logic (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

23. Referring to claim 19, Bosshart has taught wherein said mode detection logic, upon execution of said native branch macro instruction, directs said translation logic to cease decoding said macro instructions (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

24. Referring to claim 21, Bosshart has taught where said target address is provided in an architectural register (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

25. Referring to claim 22, Bosshart has taught wherein said instruction router routes the micro instructions from a macro instruction bus to a micro instruction bus (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

26. Referring to claim 23, Bosshart has taught wherein said mode detection logic, upon execution of said native branch return macro instruction, directs said translation logic to resume decoding said macro instructions (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4, line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

27. Referring to claim 24, Bosshart has taught wherein said return address designates a next macro instruction, said next macro instruction being one of said macro instructions (Rosshart column 1, lines 17-37; column 1, line 53 to column 2, line 14; column 2, line 46 to column 4,

line 39; column 7, lines 36-42; column 8, line 61 to column 9, line 12; column 9, lines 24-37; Figure 1; Figure 2; Figure 5; Figure 6; and Figure 8).

***Response to Arguments***

28. Applicant's arguments with respect to claims 1-19 and 21-24 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Gruno et al., U.S. Patent Number 4,156,900, has taught a microinstruction sequence with branch instructions.

b. Amdahl, U.S. Patent Number 4,245,302, has taught microinstruction sequences for executing a target instruction.

c. Narita et al., U.S. Patent Number 5,148,532, has taught a micro-ROM storing microinstructions that execute a macroinstruction.

d. Zaidi et al., U.S. Patent Number 5,396,634, has taught executing macroisntructions using microisntructions.

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

31. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL

Aimee J. Li
March 19, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

# REVISED AMENDMENT PRACTICE: 37 CFR 1.121 CHANGED COMPLIANCE IS MANDATORY - Effective Date: July 30, 2003

All amendments filed on or after the effective date noted above must comply with revised 37 CFR 1.121. See Final Rule: **Changes To Implement Electronic Maintenance of Official Patent Application Records** (68 *Fed. Reg.* 38611 (June 30, 2003), posted on the Office's website at: http://www.uspto.gov/web/patents/ifw/ with related information. The amendment practice set forth in revised 37 CFR 1.121, and described below, replaces the voluntary revised amendment format available to applicants since February 2003. **NOTE: STRICT COMPLIANCE WITH THE REVISED 37 CFR 1.121 IS REQUIRED AS OF THE EFFECTIVE DATE (July 30, 2003).** The Office will notify applicants of amendments that are not accepted because they do not comply with revised 37 CFR 1.121 via a Notice of Non-Compliant Amendment. See MPEP 714.03 (Rev. 1, Feb. 2003). The non-compliant section(s) will have to be corrected and the entire corrected section(s) resubmitted within a set period.

***Bold underlined italic font has been used below to highlight the major differences between the revised 37 CFR 1.121 and the voluntary revised amendment format that applicants could use since February, 2003.***
Note: The amendment practice for **reissues** and **reexamination proceedings**, except for drawings, has not changed.

## REVISED AMENDMENT PRACTICE

**I. Begin each section of an amendment document on a separate sheet:**
Each section of an amendment document (*e.g.*, Specification Amendments, Claim Amendments, Drawing Amendments, and Remarks) must begin on a separate sheet. Starting each separate section on a new page will facilitate the process of separately indexing and scanning each section of an amendment document for placement in an image file wrapper.

**II. Two versions of amended part(s) no longer required:**
**37 CFR 1.121 has been revised to no longer require two versions (a clean version and a marked up version) of each replacement paragraph or section, or amended claim. Note, however, the requirements for a clean version and a marked up version for substitute specifications under 37 CFR 1.125 have been retained.**

**A) Amendments to the claims:**
Each amendment document that includes a change to an existing claim, cancellation of a claim or submission of a new claim, **must include a complete listing** of all claims in the application. After each claim number in the listing, the status must be indicated in a parenthetical expression, and **the text of each pending claim** (with markings to show current changes) must be presented. The claims in the listing will replace all prior claims in the application.

(1) The current status of all of the claims in the application, including any previously canceled, not entered or withdrawn claims, must be given in a parenthetical expression following the claim number using only one of the following seven status identifiers: (original), (currently amended), (canceled), (withdrawn), (new), ***(previously presented) and (not entered).*** The text of all pending claims, ***including withdrawn claims,*** must be submitted each time any claim is amended. Canceled ***and not entered*** claims must be indicated by only the claim number and status, without presenting the text of the claims.

(2) The text of all claims being currently amended must be presented in the claim listing with markings to indicate the changes that have been made relative to the immediate prior version. The changes in any amended claim must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as).* An accompanying clean version is not required and should not be presented. Only claims of the status "currently amended," and "withdrawn" that are being amended, may include markings.

(3) The text of pending claims not being currently amended, ***including withdrawn claims,*** must be presented in the claim listing in clean version, *i.e.*, without any markings. Any claim text presented in clean version will constitute an assertion that it has not been changed relative to the immediate prior version except to omit markings that may have been present in the immediate prior version of the claims.

(4) A claim being canceled must be listed in the claim listing with the status identifier "canceled"; the text of the claim must not be presented. Providing an instruction to cancel is optional.
(5) Any claims added by amendment must be presented in the claim listing with the status identifier "(new)"; the text of the claim must not be underlined.
(6) All of the claims in the claim listing must be presented in ascending numerical order. Consecutive canceled, or not entered, claims may be aggregated into one statement (*e.g.*, Claims 1 – 5 (canceled)).

**Example of listing of claims (use of the word "claim" before the claim number is optional):**

Claims 1-5 (canceled)

Claim 6 (previously presented): A bucket with a handle.

Claim 7 (withdrawn): A handle comprising an elongated wire.

Claim 8 (withdrawn): The handle of claim 7 further comprising a plastic grip.

Claim 9 (currently amended): A bucket with a ~~green~~ blue handle.

Claim 10 (original): The bucket of claim 9 wherein the handle is made of wood.

Claim 11 (canceled)

Claim 12 (not entered)

Claim 13 (new): A bucket with plastic sides and bottom.

**B) Amendments to the specification:**
Amendments to the specification, including the abstract, must be made by presenting a replacement paragraph or section or abstract marked up to show changes made relative to the immediate prior version. An accompanying clean version is not required and should not be presented. Newly added paragraphs or sections, including a new abstract (instead of a replacement abstract), must not be underlined. A replacement or new abstract must be submitted on a separate sheet, 37 CFR 1.72. If a substitute specification is being submitted to incorporate extensive amendments, both a clean version (which will be entered) and a marked up version must be submitted as per 37 CFR 1.125.

The changes in any replacement paragraph or section, or substitute specification must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as)*

**C) Amendments to drawing figures:**
Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment, ***and may be accompanied by a marked-up copy of one or more of the figures being amended, with annotations.*** Any replacement drawing sheet must ***be identified in the top margin as "Replacement Sheet"*** and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. ***Any marked-up (annotated) copy showing changes must be labeled "Annotated Marked-up Drawings" and accompany the replacement sheet in the amendment (e.g., as an appendix).*** The figure or figure number of the amended drawing(s) must **not** be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Questions regarding the submission of amendments pursuant to the revised practice set forth in this flyer should be directed to: Elizabeth Dougherty or Gena Jones, Legal Advisors, or Joe Narcavage, Senior Special Projects Examiner, Office of Patent Legal Administration, by e-mail to patentpractice@uspto.gov or by phone at (703) 305-1616.